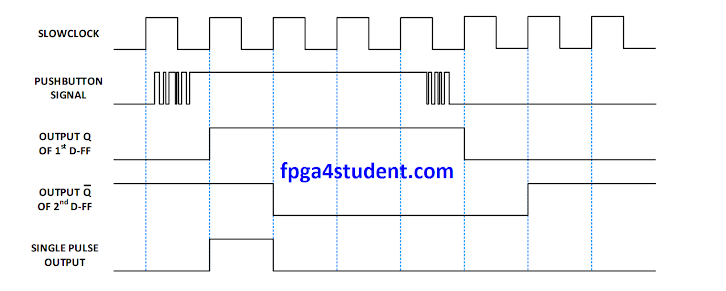
Lab 5: Introduction to FPGA, Verilog and State Machines – Blinking LEDs and Button Input

Steps Involved:

1. Taking Input:
   * Basys 3 clock runs at 100MHz. At each clock cycle, multiple button presses are recorded for a single button press, in addition to unpredictable electrical noise causing worse results. Consequently, a debouncing technique is needed for the preservation of a clean pulse signal that records a button press.



* + Debouncing is done through the creation of a slower local clock within a debouncing module, and the introduction of a delay of 3 such slow clock cycles for the button to stabilize before a high input is recorded (this approach may vary by student).

1. Delay:
   * Button presses serve to increase the delay of the system, or to reset it.
   * The default delay may be of one second, after which each button press may increase the delay by one second also.
   * The system may constantly check for a button press at every clock cycle, and increment or reset it as fit.
2. Counter:
   * A counter runs with an initial of 0, incrementing at each clock cycle.
   * The maximum value of this counter is determined by the delay set, with the default delay causing a maximum of 512 (can be configured to something else), and further increment in the delay reduces the maximum value of count; all such that the total runtime of the counter from its initial state to its maximum value remains constant.
   * This may be calculated by:

runtime = 512s

clock cyles of runtime = runtime x clock cycles per second

= 512 x 10^8

maxCount = runtime / delay

= 512 / delay

* Once it reaches the maximum value or if reset is pressed before this, the counter resets to 0.
* At every increment, the counter generates a pulse signal to indicate a counter increment.

1. Output through Seven Segment:
   * The seven-segment pattern is operated using a state machine.
   * Seven-segments use common anodes and common cathodes. As a result, at no point in time may all the digits light up at the same time.
   * This introduces the concept of persistence of vision, wherein the blink pattern of switching between the four digits blinking must be so fast that it will *feel* as if they are all on at the same time, even though that is not the case.
   * As a result, you need a state machine to vary the loop of the digit index selected to be lit up at a time, and a counter to monitor the delay between a digit index switch.
   * The digits may then display 4 bits of the count value corresponding to their index, and the full number is thus displayed on the display.